AMENDMENT TO THE SPECIFICATION

Please add the following paragraphs on page 1, line 5 (after the paragraph that ends "filed February 11, 2003, which is hereby incorporated by reference." and before the paragraph that begins "The following 23 documents....")

BACKGROUND

Field of the Invention

This invention is directed to a chip-level architecture used in combination with a monolithic three-dimensional write-once memory array.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a drawing labeled "Agenda."

Figure 2 is a drawing labeled "Memory Cell (1/3)."

Figure 3 is a drawing labeled "Memory Cell (2/3)."

Figure 4 is a drawing labeled "Memory Cell (3/3)."

Figure 5 is a drawing labeled "Process Highlights."

Figure 6 is a drawing labeled "Array of Stacked Memory Cells."

Figure 7 is a drawing labeled "Connections to the Array."

Figure 8 is a drawing labeled "Tile Organization."

Figure 9 is a drawing labeled "Die Organization (1/3)."

Figure 10 is a drawing labeled "Die Organization (2/3)."

Figure 11 is a drawing labeled "Die Organization (3/3)."

Figure 12 is a drawing labeled "Fault Tolerance."

Figure 13 is a drawing labeled "Chip Block Diagram."

Figure 14 is a drawing labeled "Write Operation (1/2)."

Figure 15 is a drawing labeled "Write Operation (2/2)."

Figure 16 is a drawing labeled "Read Operation."

Figure 17 is a drawing labeled "Read Sense Amplifier."

Figure 18 is a drawing labeled "Sensing IREAD=300nA."

Figure 19 is a drawing labeled "Vread Generator."

Figure 20 is a drawing labeled "Vread Generator."

Figure 21 is a drawing labeled "Bit Area Comparison."

Figure 22 is a drawing labeled "Device Characteristics."

Figure 23 is a drawing labeled "Summary."

Detailed Description of the Presently Preferred Embodiments

Please replace the paragraph on page 1, lines 9-10 with the following amended paragraph:

2. 23 pages of slides (first slide labeled "Agenda;" last slide labeled "Summary"), which are reproduced herein as Figures 1-23.

Please replace the paragraphs on page 1, line 15 – page 3, line 10 with the following amended paragraphs:

5. U.S. Patent ~~Application Serial~~ No. ~~09/928,536~~ 6,525,953 to Johnson ("Vertically-Stacked, Field Programmable, Nonvolatile Memory and Method of Fabrication").

6. U.S. Patent ~~Application Serial~~ No. ~~10/185,507~~ 6,952,043 to Vyvoda et al. ("Electrically Isolated Pillars in Active Devices").

7. U.S. Patent Application Serial No. 10/326,470 to Herner et al. ("An Improved Method for Making High-Density Nonvolatile Memory").

8. U.S. Patent Application ~~Serial~~ Publication No. ~~09/748,589~~ US 2003-0120858 A1 to March et al. ("Memory Devices and Methods for Use Therewith").

9. U.S. Patent ~~Application Publication~~ No. ~~US 2002-0081782 A1~~ 6,534,403 ("Contact and Via Structure and Method of Fabrication").

10. U.S. Patent ~~Application Publication~~ No. ~~US 2002-0136076 A1~~ 6,574,145 ("Memory Device and Method for Sensing while Programming a Non-Volatile Memory Cell").

11. U.S. Patent ~~Application Publication~~ No. ~~US 2002-0136045 A1~~ 6,567,287 ("Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern under a Plurality of Memory Arrays").

12. U.S. Patent ~~Application Serial~~ No. ~~10/024,647~~ 6,928,590 ("Memory Device and Method for Storing Bits in Non-Adjacent Storage Locations in a Memory Array").

13. U.S. Patent Application ~~Serial~~ Publication No. ~~10/024,646~~ US 2003-0115518 A1 ("Memory Device and Method for Redundancy/Self-Repair").

14. U.S. Patent ~~Application Publication~~ No. ~~US 2002-0083390-A1~~ 6,591,394 ("Three-Dimensional Memory Array and Method for Storing Data Bits and ECC Bits Therein").

15. U.S. Patent No. 6,486,728 to Kleveland ("Multi-Stage Charge Pump").

16. U.S. Patent No. 6,385,074 to Johnson et al. ("Integrated Circuit Structure Including Three-Dimensional Memory Array").

17. U.S. Patent ~~Application Serial~~ No. ~~09/748,649~~ 6,661,730 to Scheuerlein et al. ("Partial Selection of Passive Element Memory Cell Sub-Arrays for Write Operation").

18. (a) U.S. Patent ~~Application Publication~~ No. ~~US 2002-0136047A1~~ 6,618,295 to Scheuerlein ("Method and Apparatus for Biasing Selected and Unselected Array Lines when Writing the Memory Array"). (b) U.S. Patent No. 6,504,753, which has the same specification (excluding the claims).

19. (a) U.S. Patent Application Serial No. 09/896,468 to Scheuerlein ("Current Sensing Method and Apparatus Particularly Useful for a Memory Array of Cells Having Diode-Like Characteristics"). (b) U.S. Patent ~~Application Serial~~ No. ~~09/897,704~~ 6,522,594 to Scheuerlein ("Memory Array Incorporating Noise Detection Line"), which has the same specification (excluding the claims).

20. U.S. Patent No. 6,407,953 to Cleeves et al. ("Memory Array Organization and Related Test Method Particular Well Siuted for Integrated Circuits Having Write Once Memory Arrays").

21. U.S. Patent No. 6,515,904 to Moore et al. ("Method and System for Increasing Programming Bandwidth in a Non-Volatile Memory Device").

22. U.S. Patent ~~Application Serial~~ No. ~~10/306,887~~ 6,856,572 to Scheuerlein et al. ("Multiheaded Decoder Structure Utilizing Memory Array Line Driver with Dual Purpose Driver Device ").

23. U.S. Patent ~~Application Serial~~ No. ~~10/217,182~~ 6,781,878 to Kleveland et al. ("A Dynamic Sub Array Group Selection Scheme").

Please replace the paragraph on page 3, lines 15-16 with the following amended paragraph:

The Chip Block Diagram in the above-listed document number 2, which is reproduced herein as Figure 13, exemplifies a preferred embodiment of the architecture showing the functional organization of:

Please replace the paragraph on page 3, line 22 with the following amended paragraph:

a Vread Generator exemplified in document 2 above with a circuit schematic (see Figures 19-20 herein);

Please replace the paragraph on page 4, line 17 – page 5, line 2 with the following amended paragraph:

The sub arrays have read and write sensing circuitry connected to array lines in one direction (i.e., sensing lines). The circuitry is shared between adjacent subarrays by the method described for checkerboard arrays. The circuitry uses current sensing methods and noise cancellation lines described in documents 18 and 19, particularly the sensing circuit shown in the Read Sense Amplifier figure of document 2 (which is reproduced herein as Figure 17) and described in document 1, to allow large sub arrays with reliable sensing. All the sensing circuits for subarrays in a column are connected together by means of shared bi-directional data busses and control lines on a layer of interconnection metal above the memory cells. The data busses and control lines are preferably substantially parallel to one another and parallel to the sensing lines in the memory array. They connect the sub arrays to control circuitry in the smart write controller. The data bus is bi-directionally controlled in both read and write operations to reduce the number of wires required. The smart write controller transfers data between the selected memory sub arrays and a register called a page register/ fault memory during read and write operations. Thereby, the data from the page register is written to or read from a set of cells distributed across all the selected sub arrays.

Please replace the paragraph on page 5, line 27 – page 6, line 2 with the following amended paragraph:

Each memory line has two control transistors, as shown in document 2, the foil titled, "Die Organization 2/3~~,~~ which is reproduced herein as Figure 10." These are the "two transistors" referred to in the "Tile ~~Organizaton~~ Organization" foil of document 2, which is reproduced herein as Figure 8, while "epsilon" is the amortized cost of the row decoders and bias circuits. This die organization can be used alone or in combination with any other elements disclosed herein.